



01-16-04

1762

Express Mail No. EV 346 810 351 US.**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: Claire RICHTARCH

Confirmation No. 6886

Application No: 10/671,812

Group Art Unit: 1762

Filing Date: September 25, 2003

Examiner:

For: METHOD OF PREPARING A SURFACE
OF A SEMICONDUCTOR WAFER TO
MAKE IT EPIREADY

Atty. Docket No.: 4717-11300

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENTCommissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Pursuant to applicants' duty of disclosure under 37 C.F.R. 1.56, enclosed is a PTO form 1449 which lists (3) cited references for the Examiner's review and consideration. It is respectfully requested that these references be made of record in this application by the Examiner's completion and return of the PTO Form 1449.

No fee or certification is believed to be due for this submission since the filing of this statement is being submitted prior to the issuance of the first office action for this application. Should any fees be required, however, please charge such fees to **Winston & Strawn** Deposit Account No. 50-1814.

Date: _____

1/14/04

Respectfully submitted,

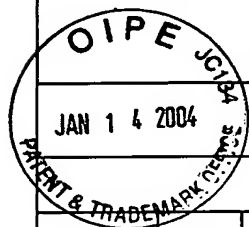
Allan A. Fanucci (Reg. No. 30,256)

**WINSTON & STRAWN LLP
CUSTOMER NO. 28765**

Enclosures

(212) 294-3311

LIST OF REFERENCES CITED BY APPLICANT Form PTO-1449 <i>(Use several sheets if necessary)</i>	ATTY. DOCKET NO.:	APPLICATION NO.:
	4717-11300	10/671,812
APPLICANT:		
Claire RICHTARCH		
FILING DATE:		GROUP:
September 25, 2003		1762



U.S. PATENT DOCUMENTS

*EXAMINE R INITIAL	CITE NO.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						

FOREIGN PATENT DOCUMENTS

AE

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AE	FR 02-09869	8/2000	France			X	
	AF							
	AG							

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AH	A. J. Auberton-Hervé et al., "Why Can SMART-CUT® Change the Future of Microelectronics?", International Journal of High Speed Electronics and Systems, Vol. 10, no. 1, 2000, pp 131-146.
	AI	"Thermal and Dopant Processes", Chapter 4, Advanced Semiconductor Fabrication Handbook, ICE, 1998
	AJ	
	AK	

EXAMINER

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with **MPEP 609**. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

AM